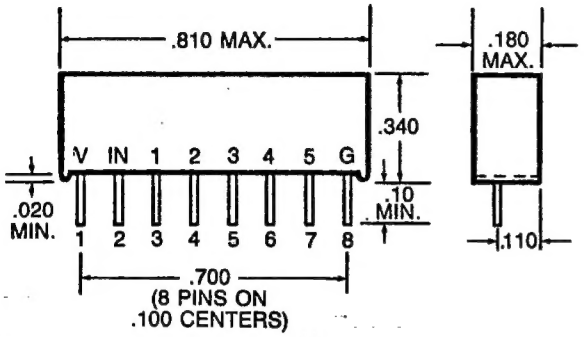
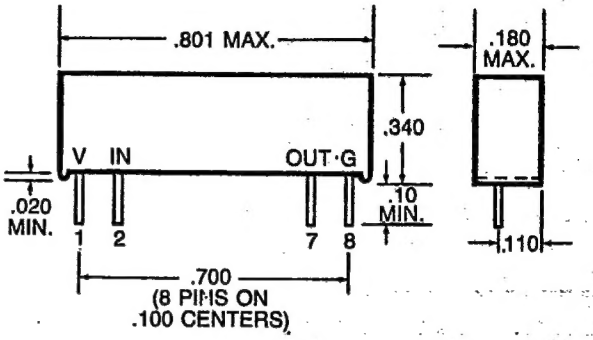
YCL

DIGITAL DELAY LINES
8 PIN SINGLE-IN-LINE PACKAGES
TTL COMPATIBLE
5 TAPS AND SINGLE OUTPUT

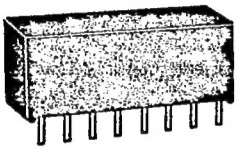
SERIES Y05 AND Y01

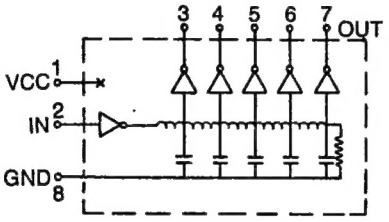


White Dot locates Pin 1

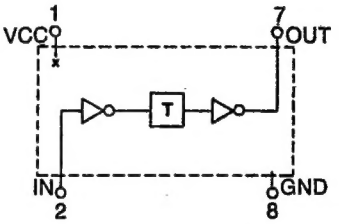


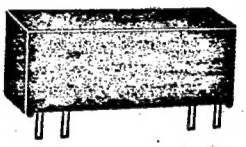
Y05





Y01





Intermediate delay values available upon request.

Model No.	TD (ns)	TD/Tap (ns)
Y05025	25	5
Y05030	30	6
Y05035	35	7
Y05040	40	8
Y05045	45	9
Y05050	50	10
Y05075	75	15
Y05100	100	20
Y05150	150	30
Y05200	200	40
Y05250	250	50
Y05300	300	60
Y05350	350	70
Y05400	400	80

Model No.	Delay (ns)
Y01010	10
Y01025	25
Y01030	30
Y01035	35
Y01040	40
Y01050	50
Y01075	75
Y01100	100
Y01150	150
Y01200	200
Y01250	250
Y01300	300
Y01350	350
Y01400	400

DC PARAMETERS		LIMITS Min.	LIMITS Max.
Voh	Vcc = min Ioh = 1.0mA	2.5V	—
Vol	Vcc = min Iol = 20mA	—	0.5V
Iih	Vcc = max Vih = 2.7V	—	50μA
Iil	Vcc = max Vil = 0.5V	−2.0mA	—
Ii	Vcc = max Vi = 5.5V	—	1.0mA
Vi	Vcc = min Iin = −18 mode	−1.2vdc	—
Icc	Vcc = max outputs low	Series Y05 70mA Series Y01 55mA	

SPECIFICATIONS:

- Supply voltage: 5.0VDC ± 5%
- Delay tolerances: ±2ns or ±5% wig
- Rise time: 4ns max
- Minimum Pulse Width: 40% of Total delay
- Maximum Duty Cycle: 50%
- Operating temp. range: 0 to 70°C
- Temp. coeff. of delays: 1.0ns +500ppm/°C
- Terminals: Electro tin plated Alloy 42 .020w × .010th

TEST CONDITIONS:

- Temperature: 25° ± 5°C; Vcc = 5.0VDC
- Input Pulse Width: 1.2 times the total delay time
- Pulse spacing: 5 times the total delay time
- Input rise time: 2ns; input pulse amplitude 3.0VDC
- All output loaded with 15pf
- Time delays measured at the 1.5 volts level on the leading edges
- Rise time measured from .75 to 2.4V